In the Claims

This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims

1. (Currently-Amended) A method to form MOS gates in an integrated circuit device comprising:

forming a dielectric layer overlying a substrate;

forming a polysilicon layer overlying said dielectric layer;

forming a silicon oxide layer overlying said polysilicon layer;

forming a patterned masking layer overlying and selectively exposing said silicon oxide layer;

thereafter oxidizing said polysilicon layer to increase thickness of said exposed silicon oxide layer wherein said thickened silicon oxide layer encroaches under the edges of said masking layer and wherein said silicon oxide layer does not thicken under other interior areas of said masking layer;

thereafter removing said masking layer;

thereafter etching said silicon oxide layer to selectively expose said polysilicon layer where said silicon oxide layer did not thicken; and

thereafter etching through said exposed polysilicon layer to thereby form MOS gates in the manufacture of said integrated circuit device

wherein before oxidizing said polysilicon layer, said silicon oxide layer is not etched through.

2. (Original) The method according to claim 1 wherein said MOS gates comprise floating gates for split gate flash devices.

3. (Original) The method according to claim 1 wherein said step of forming a silicon oxide layer comprises thermal oxidation of said polysilicon layer.

4. (Original) The method according to claim 1 wherein said step of thereafter etching said silicon oxide layer to selectively expose said polysilicon layer comprises an oxide dip.

5. (Original) The method according to claim 1 wherein said MOS gates have a dish-shaped cross-sectional profile.

6. (Original) The method according to claim 1 wherein said masking layer comprises silicon nitride.

7. (Original) The method according to claim 1 wherein edges of said MOS gates overlie isolation structures in said substrate.

8. (Original) A method according to claim 1 further comprising:

removing said silicon oxide layer after said step of etching through said exposed polysilicon layer;

thereafter etching said MOS gates to selectively expose said substrate;

thereafter forming a second dielectric layer overlying said MOS gates and said exposed substrate;

depositing a second conductor layer overlying said second dielectric layer; and

etching back said second conductor layer to form second MOS gates on sidewalls of said MOS gates.

9. (Original) The method according to claim 8 wherein said second MOS gates comprise control gates for split gate flash devices.

10. (Original) A method to form split gate flash devices in an integrated circuit device comprising:

forming a dielectric layer overlying a substrate;

forming a polysilicon layer overlying said dielectric layer;

forming a silicon oxide layer overlying said polysilicon layer;

forming a patterned masking layer overlying and selectively exposing said silicon oxide layer;

thereafter oxidizing said polysilicon layer to increase thickness of said exposed silicon oxide layer wherein said thickened silicon oxide layer encroaches under the edges of said masking layer and wherein said silicon oxide layer does not thicken under other interior areas of said masking layer;

thereafter removing said masking layer;

thereafter etching said silicon oxide layer to selectively expose said polysilicon layer where said silicon oxide layer did not thicken;

etching through said exposed polysilicon layer to thereby form floating gates;

thereafter removing said silicon oxide layer;

thereafter etching said floating gates to selectively expose said substrate;

thereafter forming a second dielectric layer overlying said floating gates and said exposed substrate;

depositing a conductor layer overlying said second dielectric layer; and

etching back said conductor layer to form control gates on sidewalls of said floating gates in the formation of said split gate flash devices in the manufacture of said integrated circuit device.

11. (Original) The method according to claim 10 wherein said step of forming a silicon oxide layer comprises thermal oxidation of said polysilicon layer.

12. (Original) The method according to claim 10 wherein said second conductor layer comprises polysilicon.

13. (Original) The method according to claim 10 wherein said step of thereafter etching said silicon oxide layer to selectively expose said polysilicon layer comprises an oxide dip.

14. (Original) The method according to claim 10 wherein said floating gates have a dish-shaped cross-sectional profile.

15. (Original) The method according to claim 10 wherein edges of said floating gates overlie isolation structures in said substrate.

16. – 20. Canceled.

21. (New) A method to form MOS gates in an integrated circuit device comprising:

forming a dielectric layer overlying a substrate;

forming a polysilicon layer overlying said dielectric layer;

forming a patterned masking layer overlying said polysilicon layer, said patterned masking layer having an opening;

oxidizing through said opening said polysilicon layer to form a first silicon oxide layer at the bottom of said opening, wherein said first silicon oxide layer encroaches under the edges of said masking layer;

removing said masking layer after formation of said first silicon oxide layer and exposing said polysilicon layer;

etching through said exposed polysilicon layer and using said first silicon oxide layer as a mask to thereby form MOS floating gates in the manufacture of said integrated circuit device; and

removing said first silicon oxide layer after said step of etching through said exposed polysilicon layer.

22. (New) The method according to claim 21, further comprising

etching said MOS floating gates to selectively expose said substrate;

forming a second dielectric layer overlying said floating MOS gates and said exposed substrate; and

depositing a second conductor layer overlying said second dielectric layer for forming control gates.

23. (New) The method according to claim 22, further comprising:

etching back said second conductor layer to form said control gates on sidewalls of said MOS floating gates.

24. (New) The method according to claim 21, further comprising:

forming a silicon oxide layer overlying said polysilicon layer;

wherein said opening on said patterned masking layer exposes said silicon oxide layer.

25. (New) The method according to claim 24, wherein the step of oxidizing said polysilicon layer thickens said exposed silicon oxide layer to form said first silicon oxide layer while said silicon oxide layer does not thicken under other interior areas of said patterned masking layer.